ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a memory having a predetermined number of divided memory spaces, a register that stores data indicating whether a refresh operation is required or not with respect to each memory space, a row address counter that, with reference to the register, counts up an address while skipping an address requiring no refresh operation, to thereby generate an address of the memory space to be refreshed, and a refresh cycle generating circuit that with reference to the register 15, generates a refresh cycle with a cycle which varies according to the number of the memory space requiring the refresh operation.